

XRM-ADC-S4/3G

Single Channel High Speed Data Acquisition
Module

User Guide

Version 1.1

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

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Photo

1. Introduction

The XRM-ADC-S4/3G is a front panel adapter card designed principally for use with Alpha Data's ADM-XRC4 and ADM-XRC5 FPGA-based PMC cards, although some limited functionality is possible with the ADM-XP PMC card.

The XRM-ADC-S4/3G is based on the ADC083000 from National Semiconductor and provides a single channel of analogue to digital conversion with 8 bit resolution at sampling rates up to 3.0 GHz. It is aimed at applications such as IF/Baseband Signal Sampling.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock.

An auxiliary I/O port is provided for use as a trigger input and general purpose signalling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.

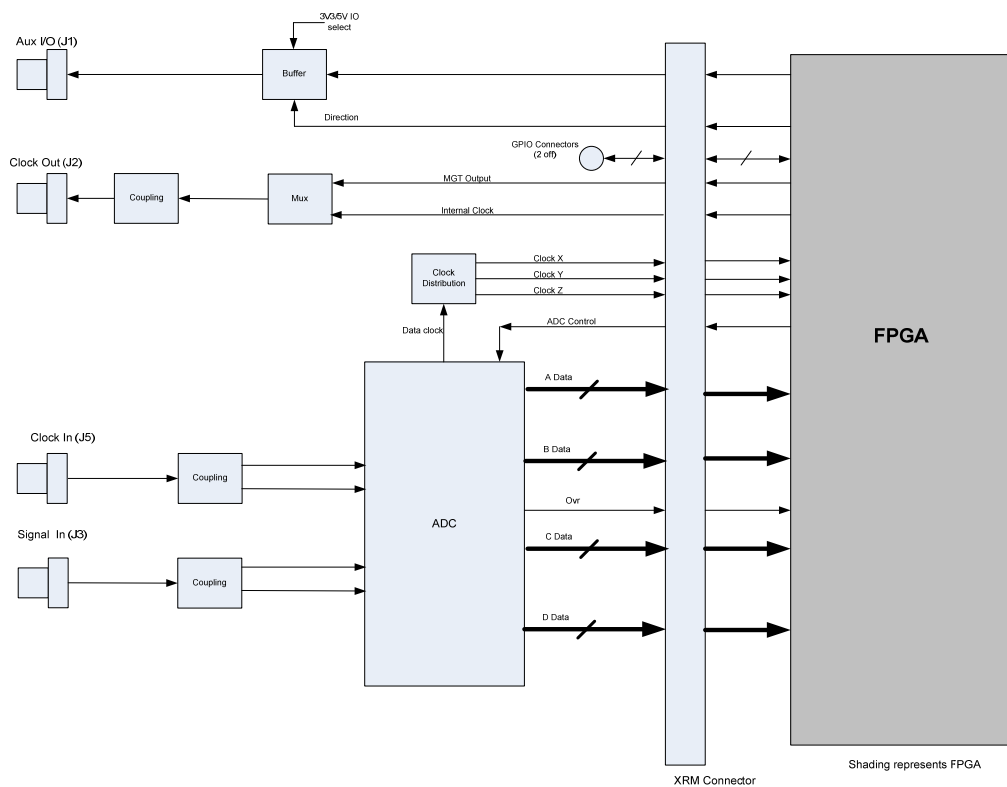


Figure 1 XRM Block Diagram

2. Installation

The XRM-ADC-S4/3G is designed to plug in to the front panel connector (SAMTEC QSH series) on the XRC series of cards. The retaining screws should be tightened to secure the XRM-ADC-S4/3G.

Note: This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3. Specification

3.1. Inputs

3.1.1. Signal (J4)

Input:	50 Ohms
Bandwidth:	30 MHz to 1700 MHz nominal
Level (Range1):	+/- 410 mV nominal
Level (Range2):	+/- 300 mV nominal

Range selectable via FPGA and ADC serial port; bandwidth limited by input transmission-line transformer. ADC 3dB bandwidth is 3GHz.

Note: exceeding the maximum input signal limit may result in permanent degradation of converter performance.

3.1.2. Clock In (J3)

Input:	50 Ohms, ac coupled
Level:	+/- 500 mV nominal. +/- 200 mV minimum to +/1V maximum
Clock Rate:	500 MHz to 1700 MHz (doubled internally by the ADC)

Note: exceeding the maximum voltage limit may result in permanent degradation of converter performance.

3.2. Input /Output

3.2.1. Clock Out (J2)

Impedance:	50 Ohms, ac coupled
Level:	+/- 400 mV nominal.
Source:	GTP or User Clock from XRC board.
Clock Rate:	20 MHz to 500 MHz , User Clock 300 MHz to 1500 MHz GTP

3.2.2. Aux IO Port (J1)

User configurable as input or output	
Input:	4k7 Ohms, dc coupled
Level:	+3V3 LVTTTL or +5V TTL (factory/user selectable ¹)

¹ configured via 0R links

3.2.3. Synch Ports (J6 and J7)

User configurable as input or output, direct to FPGA pins.

Input: dc coupled

Level: 2V5 logic

Note: signals on these connectors must be restricted to 2V5 logic levels else damage may result.

4. Options

4.1. Connector type

- SMA (7 mm, standard)
- Long Barrel SMA (20 mm)
- SMB
- SMC

4.2. Order Code

XRM-ADC-S4/3G –[Connector option] –[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option. For custom filter designs or other customisation requirements (e.g. connectors) please contact Alpha Data.

5. Related Documents

ADM-XRC4SX User Manual
ADM-XRC4LX User Manual
ADM-XMC4FX User Manuals
ADM-XRC5LX User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual

ADM-XP User Manual

6. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

7. Pinout

Pin No.	UCF Name	XRC 4SX	XRC 4LX	XMC 4FX	ADPE 4FX
18	adc_psuen	K28	K28	J26	J36
1	tmon_alert_l	H28	H28	C27	F35
3	tmon_temp_data	H27	H27	C28	G35
5	tmon_temp_ck	K27	K27	L29	F36
7	adc_cntrl_oe_l	J27	J27	K29	G36
9	adc_cntrl_pwdnq	H30	H30	F28	E34
10	adc_cntrl_cal	J30	J30	F29	D37
12	adc_cntrl_pwdn	J29	J29	E29	E37
11	adc_cntrl_cal_active	H29	H29	E28	F34
2	adc_cntrl_scs_l	D32	D32	L28	C34
4	adc_cntrl_sck	C32	C32	K28	D34
6	adc_cntrl_sdata	N22	N22	J29	D36
25	mux_sel<1>	L34	L34	F31	V25
27	mux_sel<0>	L33	L33	G31	W26
30	auxio_dirn	L28	L28	L31	V27
36	auxio	M27	M27	F33	R32
38	gpio_p	F33/D34	F33/D34	C25/F25	M35/N35
40	gpio_n	F34/E34	F34/E34	D25/F24	L35/N34
89	adc_ckx_p	AC32/AD34	R32/P34	E32/M28	U33/T30
91	adc_ckx_n	AC33/AC34	R33/R34	D32/M27	U32/T29
97	adc_cky_p	AK24/AL24	AG30/AF29	T35/U36	AD29/AE36
99	adc_cky_n	AJ24/AL25	AG31/AF30	T34/T36	AE29/AD36
102	adc_ckz_p	AN22/AM21	AC28/AA25	V37/V35	AE32/AF35
104	adc_ckz_n	AN23/AM22	AB28/AA26	U37/U35	AD32/AG35
88	adc_ovr_p	AE32	R31	N32	V35
86	adc_ovr_n	AD32	T31	M32	U35
82	Cdata_p<0>	AC28	N32	J37	W32
84	Cdata_n<0>	AB28	P32	J36	Y33
100	Cdata_p<1>	AF31	U30	H37	W30
98	Cdata_n<1>	AE31	U31	G37	W29
103	Cdata_p<2>	AJ34	U32	N33	AA26
101	Cdata_n<2>	AH34	U33	M33	Y26
121	Cdata_p<3>	AG30	V23	R32	AA36
123	Cdata_n<3>	AG31	V24	P32	AB36
122	Cdata_p<4>	AH32	W32	R31	Y32
124	Cdata_n<4>	AH33	V32	T31	Y31
126	Cdata_p<5>	AM32	Y29	U33	AB28
128	Cdata_n<5>	AM33	W29	U32	AB27
136	Cdata_p<6>	AJ30	Y28	V30	AA28
134	Cdata_n<6>	AH30	Y27	V29	Y27
140	Cdata_p<7>	AP27	AJ34	N37	AF33
138	Cdata_n<7>	AN27	AH34	M37	AE33
147	Adata_p<0>	AK21	AE33	R37	AE37
145	Adata_n<0>	AL21	AE34	P37	AD37
135	Adata_p<1>	AM31	AB31	W26	AB26
133	Adata_n<1>	AL31	AA31	V25	AB25
127	Adata_p<2>	AK33	W27	M35	AB23
125	Adata_n<2>	AK34	V27	L35	AA23
129	Adata_p<3>	AB22	AB32	U31	AA35
131	Adata_n<3>	AB23	AB33	U30	AB35
141	Adata_p<4>	AP21	AA23	K37	AD35
143	Adata_n<4>	AP22	AA24	K36	AD34
146	Adata_p<5>	AF26	AB30	W36	AF31
148	Adata_n<5>	AE26	AA30	Y36	AG31
144	Adata_p<6>	AK29	AA28	R36	AC30
142	Adata_n<6>	AJ29	AA29	P36	AC29

130	Adata_p<7>	AL33	AA33	V28	AA31
132	Adata_n<7>	AL34	AA34	U28	AA30
175	Ddata_p<0>	AG23	AM32	AB28	AL35
173	Ddata_n<0>	AF24	AM33	AB27	AM35
180	Ddata_p<1>	AL23	AM31	AA28	AF30
178	Ddata_n<1>	AM23	AL31	Y27	AG30
176	Ddata_p<2>	AL26	AK33	AB26	AM33
174	Ddata_n<2>	AK26	AK34	AB25	AN33
172	Ddata_p<3>	AP24	AB22	AA31	AK33
170	Ddata_n<3>	AN24	AB23	AA30	AK32
168	Ddata_p<4>	AL28	AF33	AB23	AN35
166	Ddata_n<4>	AL29	AF34	AA23	AN34
164	Ddata_p<5>	AJ27	AF31	W30	AG33
162	Ddata_n<5>	AH27	AE31	W29	AG32
156	Ddata_p<6>	AF28	W24	W35	AC28
154	Ddata_n<6>	AE27	Y24	W34	AD27
152	Ddata_p<7>	AP30	AC29	R34	AH35
150	Ddata_n<7>	AN30	AC30	P35	AJ35
161	Bdata_p<0>	AH28	AC32	AA35	AJ37
163	Bdata_n<0>	AH29	AC33	AB35	AK37
167	Bdata_p<1>	AM26	AL33	Y32	AL36
165	Bdata_n<1>	AM27	AL34	Y31	AM36
149	Bdata_p<2>	AK22	AG32	V34	AF36
151	Bdata_n<2>	AK23	AG33	V33	AG36
153	Bdata_p<3>	AP29	AD27	W32	AD31
155	Bdata_n<3>	AN29	AC27	Y33	AD30
159	Bdata_p<4>	AP25	AE29	Y34	AG37
157	Bdata_n<4>	AP26	AD29	AA34	AH37
160	Bdata_p<5>	AM30	AE32	AA36	AG28
158	Bdata_n<5>	AL30	AD32	AB36	AF28
171	Bdata_p<6>	AG25	AH32	AA26	AH34
169	Bdata_n<6>	AG26	AH33	Y26	AJ34
179	Bdata_p<7>	AN25	AJ30	Y29	AM37
177	Bdata_n<7>	AM25	AH30	AA29	AN37

Pin No.	UCF Name	XRC 5LX	XRC 5T1	XRC 5T2
18	adc_psuen	AN10	AK11	N39
1	tmon_alert_l	AL6	AP14	Y34
3	tmon_temp_data	AL5	AN14	AA34
5	tmon_temp_ck	AL4	AM13	W35
7	adc_cntrl_oe_l	AM5	AN13	Y35
9	adc_cntrl_pwdnq	AM6	AB8	P37
10	adc_cntrl_cal	AM7	AM11	U38
12	adc_cntrl_pwdn	AM8	AM12	T37
11	adc_cntrl_cal_active	AN7	AC8	R37
2	adc_cntrl_scs_l	AN4	AA10	J38
4	adc_cntrl_sck	AN5	AB10	K38
6	adc_cntrl_sdata	AP5	AA8	K40
25	mux_sel<1>	AP12	AE11	F40
27	mux_sel<0>	AP11	AF11	F39
30	auxio_dirn	AP15	AG10	AA35
36	auxio	AA8	AB6	F42
38	gpio_p	AP9	AD10	H40
40	gpio_n	AP10	AD11	J40
89	adc_ckx_p	AE8	AG5	Y39
91	adc_ckx_n	AF8	AF5	Y38
97	adc_cky_p	AA4	K8	AE40

99	adc_cky_n	AB5	K9	AD40
102	adc_ckz_p	AG1	T8	AV4
104	adc_ckz_n	AG2	U7	AU39
88	adc_ovr_p	AD11	V10	N40
86	adc_ovr_n	AE11	V9	P40
82	Cdata_p<0>	AG11	V8	AA40
84	Cdata_n<0>	AF11	U8	AA39
100	Cdata_p<1>	W9	F9	AB41
98	Cdata_n<1>	Y9	F8	AB42
103	Cdata_p<2>	Y11	E9	AC40
101	Cdata_n<2>	W11	E8	AC39
121	Cdata_p<3>	W10	F10	AJ42
123	Cdata_n<3>	V10	G10	AJ41
122	Cdata_p<4>	V9	G8	AC41
124	Cdata_n<4>	V8	H8	AD42
126	Cdata_p<5>	Y7	D12	AB39
128	Cdata_n<5>	Y8	C12	AC38
136	Cdata_p<6>	AB6	B13	AG42
134	Cdata_n<6>	AC5	C13	AH41
140	Cdata_p<7>	AF5	F11	AF41
138	Cdata_n<7>	AE6	E11	AF42
147	Adata_p<0>	AK4	N10	AP42
145	Adata_n<0>	AJ5	N9	AP41
135	Adata_p<1>	Y4	J10	AT41
133	Adata_n<1>	W4	J9	AU41
127	Adata_p<2>	W5	K11	AR42
125	Adata_n<2>	V5	J11	AT42
129	Adata_p<3>	Y6	H10	AL41
131	Adata_n<3>	W6	H9	AK42
141	Adata_p<4>	AH4	M10	AU42
143	Adata_n<4>	AJ4	L9	AV41
146	Adata_p<5>	W1	N8	AE39
148	Adata_n<5>	V2	N7	AE38
144	Adata_p<6>	AF6	E12	AB37
142	Adata_n<6>	AG6	E13	AB38
130	Adata_p<7>	AA6	A13	AE42
132	Adata_n<7>	AA5	B12	AD41
175	Ddata_p<0>	AL1	T10	AC36
173	Ddata_n<0>	AM1	T11	AD35
180	Ddata_p<1>	AM3	E6	AR40
178	Ddata_n<1>	AN3	E7	AT40
176	Ddata_p<2>	AN2	G6	AN40
174	Ddata_n<2>	AP2	G7	AP40
172	Ddata_p<3>	AG3	F5	AJ38
170	Ddata_n<3>	AH3	F6	AK39
168	Ddata_p<4>	AF3	H7	AL39
166	Ddata_n<4>	AE3	J7	AM39
164	Ddata_p<5>	AE2	J6	AJ37
162	Ddata_n<5>	AD2	J5	AH38
156	Ddata_p<6>	W2	N5	AF39
154	Ddata_n<6>	Y1	P5	AG38
152	Ddata_p<7>	AG5	F13	AH40
150	Ddata_n<7>	AH5	G13	AJ40
161	Bdata_p<0>	AC2	R6	AM37
163	Bdata_n<0>	AD1	T6	AL37
167	Bdata_p<1>	AF1	R7	AD36
165	Bdata_n<1>	AE1	R8	AD37
149	Bdata_p<2>	V4	M6	AN39
151	Bdata_n<2>	V3	M5	AP38
153	Bdata_p<3>	Y3	M7	AT39
155	Bdata_n<3>	Y2	L6	AR39
159	Bdata_p<4>	AB1	P7	AG37
157	Bdata_n<4>	AA1	P6	AF37
160	Bdata_p<5>	AB3	K7	AN38
158	Bdata_n<5>	AA3	K6	AM38
171	Bdata_p<6>	AK2	H5	AC35

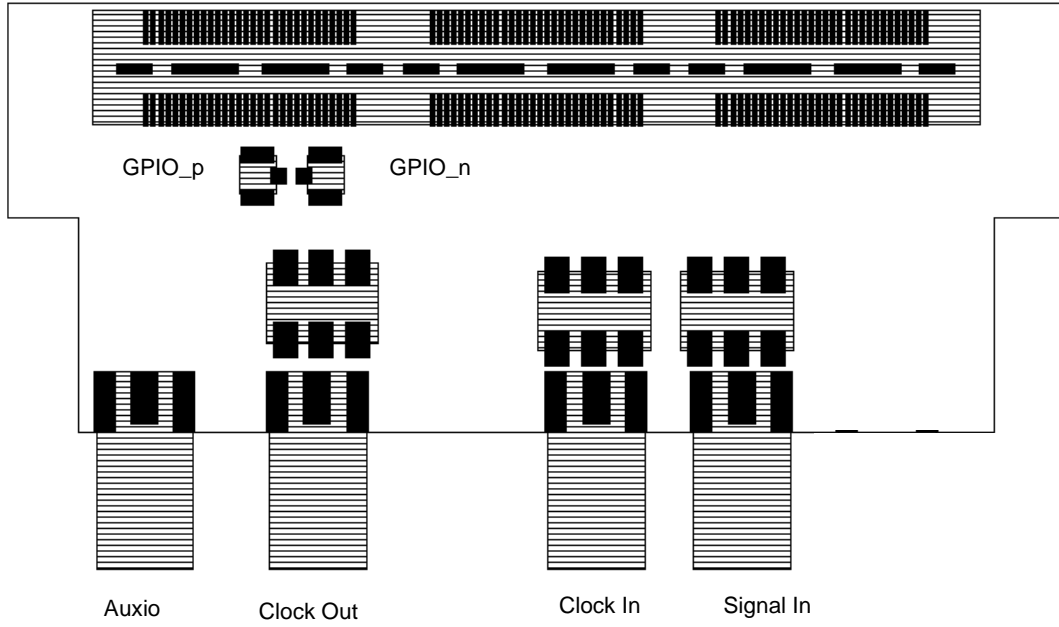
169	Bdata_n<6>	AK3	G5	AB36
179	Bdata_p<7>	AM2	T9	AB34
177	Bdata_n<7>	AL3	U10	AC34

Notes:

1. Analogue data is encoded in offset binary format with 0xFF representing positive full scale and 0x00 representing negative full scale.
2. OVERRANGE goes high when the signal input is outwith the valid ADC input range.
3. Auxio is routed via a bidirectional buffer which converts FPGA logic levels to either 3V3 or 5V levels. This port defaults to an input when the FPGA is unconfigured.
4. Gpio_n and Gpio_p are connected directly to FPGA IO pins to allow fast signalling between boards. Care should be taken when using these to ensure that the correct logic levels and directions are configured otherwise permanent damage to the FPGA may result.
5. The example UCF files supersede any pinouts above.
6. Other unlisted boards may be supported - see the UCF files in the example code
7. Temperature monitoring of the DAC is provided.
8. Further information on pin functions is contained in the example code.

8. Board Layout

Samtec 180 way



Revision History

Date	Revision	Nature of Change
Dec-2007	1.0	First issue